IN THE ABSTRACT

Please amend the Abstract as follows:

~~Method and apparatus for reducing power consumption in a digital specific signal processor integrated circuit. Data buses are routed through multiplexers to reduce the number of busses routed across an integrated circuit and maintain their prior state. Global memory is clustered into memory clusters. The memory cluster having a memory block to be accessed is activated without activating other memory clusters in the global memory. Inactive data buses retain their state by use of bus state keepers. A loop buffer stores instructions within program loops to avoid memory accesses. Functional blocks can have their clocks gated instruction by instruction to lower power consumption. RISC and DSP units swap circuit activity to reduce power consumption. Local data memory is includes self-timed memory access activation and provides for off boundary access to further lower power consumption.~~

Bus state keepers to maintain a steady state of an inactive bus to conserve power. In one embodiment of the invention, the bus state keepers include a plurality of multiplexers and a plurality of flip flops. The plurality of flip flops to store a state of a bus in response to a select signal.